the present invention, the dopant ions have an implant energy of about 8 keV and a dose of about 2.0×10^{13} cm^{-3}. The dopant ions may include magnesium. The implanted dopant ions may be annealed for about 1 minute at a temperature of from about 1130° C. After the implant anneal, an activation anneal of the implanted dopant ions may be preformed for 15 minutes at a temperature of from about 700° C. in an atmosphere containing about 80 percent N_2 and 20 percent 0_2. In these embodiments, the epitaxial structure of the device may be an $Al_{0.2}Ga_{0.8}N$ layer having a thickness of about 250 Å, a AlN layer having a thickness of about 3.0 Å and a GaN layer having a thickness of about 1.4 μm on a silicon carbide substrate. FIG. **10** illustrated drain current versus gate bias for devices having different Mg implant doses. At the implant dose of 2.0×10^{13} cm^{-3} discussed above, the threshold voltage was +0.5V.

[0091] It will be understood that the values discussed above with respect to FIG. **10** are provided for example purposes only and, therefore, embodiments of the present invention are not limited to these values. For example, in some embodiments of the present invention, the dopant ions may have an implant energy of about 5 keV and a dose of about 3.0×10^{13} cm^{-2}, the dopant ions may be Zinc (Zn) and the implant may be annealed for about 1 minute at a temperature of about 1170° C. without departing from the scope of the present invention.

[0092] Referring now to FIG. **8**, a cross-section illustrating semiconductor devices according to some embodiments of the invention will be discussed. The device of FIG. **8** is similar to the device discussed above with respect to FIGS. **7**A through **7**E, but further includes dielectric sidewall spacers **630** on a sidewall of the trench **76**. The sidewall spacers **630** may be formed after the gate implant **510** discussed above is performed. The dielectric sidewall spacers **630** may have a thickness of from about 1.0 nm to about 50.0 nm. If the thickness of the sidewall spacers **630** is too thick, the gate electrode **32** when positively biased, may not accumulate mobile charge under the implanted region **510**, which may result in current choking at the gate edges.

[0093] In some embodiments, a conformal dielectric layer may be formed on the semiconductor device and the conformal dielectric layer may be etched to provide the dielectric sidewall spacers **630** on the sidewall of the trench **76**. In some embodiments of the present invention, the conformal dielectric layer may be etched using a highly anisotropic reactive ion etch of the conformal dielectric layer. Thus, when the gate is forward biased, the structure discussed above with respect to FIGS. **7**A through **7**E may provide a possible leakage path from the gate metal to the 2-DEG **33** via the non-implanted barrier **22** adjacent the gate implant region **510**. The sidewalls **630** of FIG. **8** may separate the gate metal from the non-implanted barrier layer **22**, which may substantially reduce or possibly eliminate the parasitic leakage path that may occur in embodiments discussed above with respect to FIGS. **7**A through **7**E. The device of FIG. **8** including the dielectric sidewalls **630** can therefore be biased to a higher gate voltage, which may result in a higher maximum drain current and a lower on-resistance.

[0094] Referring now to FIGS. **9**A and **9**B, cross-sections of devices according to some embodiments of the present invention will be discussed. As illustrated in FIGS. **9**A and **9**B, the gate electrode **32** is situated between the source **30** and the drain **31** contact. FIG. **9**B further illustrates the formation of a second non-conducting spacer layer **73**. The second non-conducting spacer **73** may have a thickness of from about 500 Å to about 5000 Å. The second non-conducting spacer layer **73** may be deposited after formation of the gate electrode **32**. The formation of the second non-conducting spacer layer **73** may be followed by the formation of a metal field plate **75**. The metal field plate **75** may be connected to either the gate **32** of the source **30** without departing from the scope of the present invention. Suitable materials for the field plate **75** may include, for example, Ni, Au, Al and Ti. FIG. **9**B only illustrates some embodiments of the present invention, it will be understood that other configurations and geometries of gate electrode **32** and the field plate **75** may also be possible.

[0095] Accordingly, some embodiments of the present invention provide a device with low resistance access regions combined with normally-off operation. As discussed above, some embodiments of the present invention provide an implanted region **510** in the barrier layer **22** under the gate electrode **32**. The presence of the implanted region **510** may bend the conduction band under the gate electrode **32** such that no mobile charge is present in the channel under the gate electrode at zero bias. At a positive gate bias, electrons accumulate in the channel at the interface between the barrier layer **22** and the underlying GaN buffer **20**. Since the implanted elements are predominantly located in the barrier layer **22**, and relatively low concentrations are present in the GaN buffer **20** and at the interface, the accumulated electrons may not be affected by scattering due to the implanted ions, which may provide a device having high mobility and a low on-state resistance as discussed above with respect to FIGS. **7**A through **10**. Accordingly, some embodiments of the present invention may provide normally-off operation of GaN HEMTs with performance comparable to normally-on devices.

[0096] Although certain structures of GaN HEMTs are discussed above, these structures are provided herein to provide examples only. The gate structure and/or gate implant region discussed herein in accordance with some embodiments of the present invention may be included in any HEMT having any structure that will provide a functional device without departing from the scope of the present invention.

[0097] In the drawings and specification, there have been disclosed typical embodiments of the invention, and, although specific terms have been employed, they have been used in a generic and descriptive sense only and not for purposes of limitation.

That which is claimed is:

1. A transistor, comprising:

a Group III-nitride buffer layer;

a Group III-nitride barrier layer on the Group III-nitride buffer layer;

a non-conducting spacer layer on the Group III-nitride barrier layer, the Group III-nitride barrier layer and the spacer layer defining a trench extending through the barrier layer and exposing a portion of the buffer layer;

a gate structure on the spacer layer and in the trench; and

a gate electrode on the gate structure.

2. The transistor of claim **1**, wherein the trench is further defined by the buffer layer, the transistor further comprising:

a second non-conducting spacer layer on the gate electrode and the dielectric layer; and

a field plate on the second non-conducting spacer.

3. The transistor of claim **2**, wherein the field plate is electrically coupled to a source electrode or the gate electrode.